RA9-97-020 **PATENT**

CONCLUSION:

Applicant respectfully requests that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Specification:

Paragraph beginning at line 20 of page 14 has been amended as follows:

Timing circuit 328 receives a Clock signal and subsequently provides appropriate timing signals in response to the methodology implemented by the present invention to each of CPU 312, external bus center interface ~~face~~ 330, and internal memory 332 via a Timing Control bus 338

Paragraph beginning at line 21 of page 15 has been amended as follows:

CPU 312 executes each of the instructions required during operation of the portion of CPU 210. Internal Address bus 336 and Internal Data bus 334 communicate information between execution unit 314 and a remaining portion of CPU 210. Bus control logic circuit 316 fetches instructions and operands. Each of the instructions is then decoded by instruction decode logic circuit 318 and provided to control unit 320 and sequencer 322. Control unit 320 and sequencer 322 maintain a sequence of execution of each of the instructions to most sufficiently utilize the computing capabilities of data processing system 108. Additionally, control unit 320 includes a micro-ROM memory (not shown), which provides a plurality of control information to each of execution unit 314 ~~312~~, bus control logic 316, and instruction decode logic 318 via a micro-ROM control bus 365.

Paragraph beginning at line 2 page 16 has been amended as follows:

CPU 312 executes each of the instructions required during operation of the portion of CPU 210. Internal Address bus 336 and Internal Data bus 334 communicate information between execution unit 314 and a remaining portion of CPU 210. Bus control logic circuit 316 fetches instructions and operands. Each of the instructions is then decoded by instruction decode logic circuit 318 and provided to control unit 320 and sequencer 322. Control unit 320 and sequencer 322 maintain a sequence of execution of

each of the instructions to most sufficiently utilize the computing capabilities of data processing system 108. Additionally, control unit 320 includes a micro-ROM memory (not shown), which provides a plurality of control information to each of execution unit 314, bus control logic 316, and instruction decode logic 318 via a micro-ROM control bus 365 ~~65~~.

Paragraph beginning at line 7 of page 19 has been amended as follows:

Should no query response be received in step 454, step 464 determines whether the response timer has expired. If the response timer has expired, the query count value is tested in a step 466. If the query count value is greater than the maximum number of queries (MAX_QUERYS), then this indicates that a communication connection failure occurred and the information is provided to software controlling operation of data processing system 108 in a step 468. However, if the query count value is not greater than the maximum number of queries, the query count value is incremented in a step 470. A program flow of the present invention subsequently returns to step 452.